Junior Digital Design and Verification Engineer

Description

The *semify* team works on easing the life of digital design and verification engineers for ASICs by helping them to understand and find simulation failures faster. To strengthen our development team for this versatile mission, we are searching for a Junior Digital Design and Verification Engineer.

Job description

During your work as Junior Design and Verification Engineer you will

- … implement and verify digital designs
- … develop and apply new digital design and verification methodologies
- … directly interact with customers and help them to solve their problems
- … be part of a young, dynamic and growing team committed to help our customers to succeed

Desired Skills

As an ideal candidate for the position of Junior Digital Design and Verification Engineer, you

- … are familiar with HDL description languages (SystemVerilog preferred)
- … can implement basic synchronous digital designs for ASICs or FPGAs
- … have a basic understanding of functional digital verification
- … can understand and write Python scripts (ideally experience with Jupyter-notebooks and NumPy)
- … are used to work with version control systems (Git preferred)
- … you enjoy working in a distributed team
- … you have the willingness to learn and grow

Working hours

The *semify* team is working in a flexible environment. The position is a full-time position based on a weekly working time of 38.5 hours.

Payment

This position is endowed with a monthly salary of € 2.428 based on 38.5 hours (over payment possible). The collective agreement for „Informationstechnik“ is applied.

Contact

If you are attracted by the position as a Junior Digital Design and Verification Engineer and you want to be part of an innovative and dynamic team, send your application including and application letter and a CV to the following email address: office@semify-eda.com.